means for supplying said default test instructions to said means for storing test instructions.

Claim 8 (Amended). An electronic system including an integrated circuit having a built-in self-test arrangement therein, said integrated circuit including

means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester,

means for generating default test instructions in absence of instructions from an external tester, and

means for supplying said default test instructions to said means for storing test instructions.

Claim 12 (Amended). A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level and board level testing and including means for storing a test algorithm, said method comprising steps of

discriminating a source of a test command,

providing a system level test algorithm from said BIST arrangement in absence of instructions from an external tester,

transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and

operating said BIST arrangement using said system level test algorithm.

REMARKS

Responding to the Examiner's objections of the drawings a set of formal drawings, correcting all mistakes noted, has been filed concurrently with this amendment.

Responding to the Examiner's objections to the specification the minor corrections of the

specification have been performed by this amendment. However, Applicant respectfully submits that not all criticisms represent grammatical errors or course ambiguity in the description of the present invention. Applicant points out that some of objections of the specification are arbitrary which do not form a basis for objection. Furthermore, Applicant would like to cite MPEP § 2173.02, which states that ,"Examiners ... should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirement." Additionally, the undersigned is not aware of any requirements in regard of putting reference numerals into parenthesis and would appreciate if the Examiner will provide a citation of the source of such requirement.

Claims 1-17 are currently pending in the application. By this amendment, claims 1, 8, and 12 are amended. Attached hereto is a separate sheet entitled "Clean Copy of Claims" showing a clean copy of the amended claims, and a separate sheet entitled "Clean Version of Changes to Specification" showing the clean copy of replacement paragraphs to the specification. Support for the amendments is provided in at least Figure 3 and at page 15, lines 17-19 of the present specification. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Claims 1-17 are rejected under 35 U.S.C. §102(e) as being anticipated by Schwartz (U.S. Patent 5,982,681). This rejection is respectfully traversed.

The invention provides an enhancement to a programmable memory BIST arrangement by using a default initialization capability for a programmable memory BIST arrangement. More specifically, a default initialization capability loads a default set of desired test instructions if not provided by an external tester. More specifically and preferably, the present invention discriminates tests in absence of instructions from an external tester. Special arrangements of an integrated circuit are provided by the present invention including an arrangement for receiving test instructions provided from an external tester, an arrangement for generating default test instructions, and an arrangements for supplying the default test instructions to the storage device for storing test instructions when discrimination of a source indicates external instructions are not available. This system level tests may be performed automatically while the claimed structure an method provides a port for an external tester through existing structure of a BIST.

The patent to Schwartz shows a reconfigurable built-in self test circuit wherein write data path from the built-in self test module to the embedded device includes a multiplexer which is controlled by an externally applied debugging signal. In case when the debug signal is de-asserted, the multiplexer forwards the write data from the built-in self test module to the embedded device, thereby allowing the self test to proceed in the hard wired manner. When the debug signal is asserted, the multiplexer forward external data from the user to the embedded device, thereby allowing the user to execute customized tests on the embedded device. Briefly, Schwartz teaches a method for debugging a faulty embedded memory. There is no structure in Schwartz that corresponds in any way to the means for discriminating as claimed.

The Examiner at the page 4 of the Office Action erroneously states that "a built-in self-test circuit is included and generates BIST data patterns (analogous to the default instructions in the present application)". Applicant respectfully points out that the present invention is not analogous and has certain distinguishable features related to the arrangement for a built -in self test. More particularly, the means for storing test instruction structure is not only mere storage, but generally performs a function of the port into BIST arrangement. This means that when an external tester does not provide instructions to the BIST Initialization Storage Module 210 discriminates testing and generates and loads the default instructions. (See Figure 3).

To emphasize the distinction, claims 1, 8 and 12 have been amended to incorporate the feature of discrimination of the test in absence of instructions from an external tester. Specifically, claim 1 and 8 now recites,"...means for storing test instructions including means for discriminating a source of a test command and receiving test instructions provided from an external tester...)".

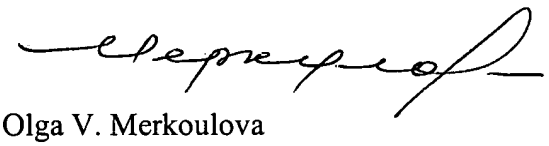
MPEP §2131 mandates that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT IN THE CLAIM". Furthermore, the MPEP, citing Richardson v. Suzuki Motor Co., 9 USPQ2d 1051, 1053 (Fed. Cir. 1987), states, "...the identical invention must be shown in as complete detail as is contained in the ...claim" (emphasis added).

Here, non of the structural limitations highlighted in Applicant's claims above are taught or suggested by Schwartz. It is therefore respectfully submitted that the rejections to the claims are improper under §102 as Schwartz cannot anticipate the rejected claims since it does not

"teach the identical invention". Based on the above discussion with reference to the MPEP guidelines, it is respectfully requested that the rejections based on 35 U.S.C. §102 be withdrawn and claims be allowed.

In view of the foregoing amendments and remarks, Applicant submits that the claims as amended are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041 (Whitham, Curtis, & Christofferson, P.C.).

Respectfully submitted,



Olga V. Merkoulova
Registration No. 48,757

Tel. (703) 391-2510 or (703) 787-9400
Fax. (703) 391-9035 or (703) 787-7557

30743
PATENT TRADEMARK OFFICE